FIG.1

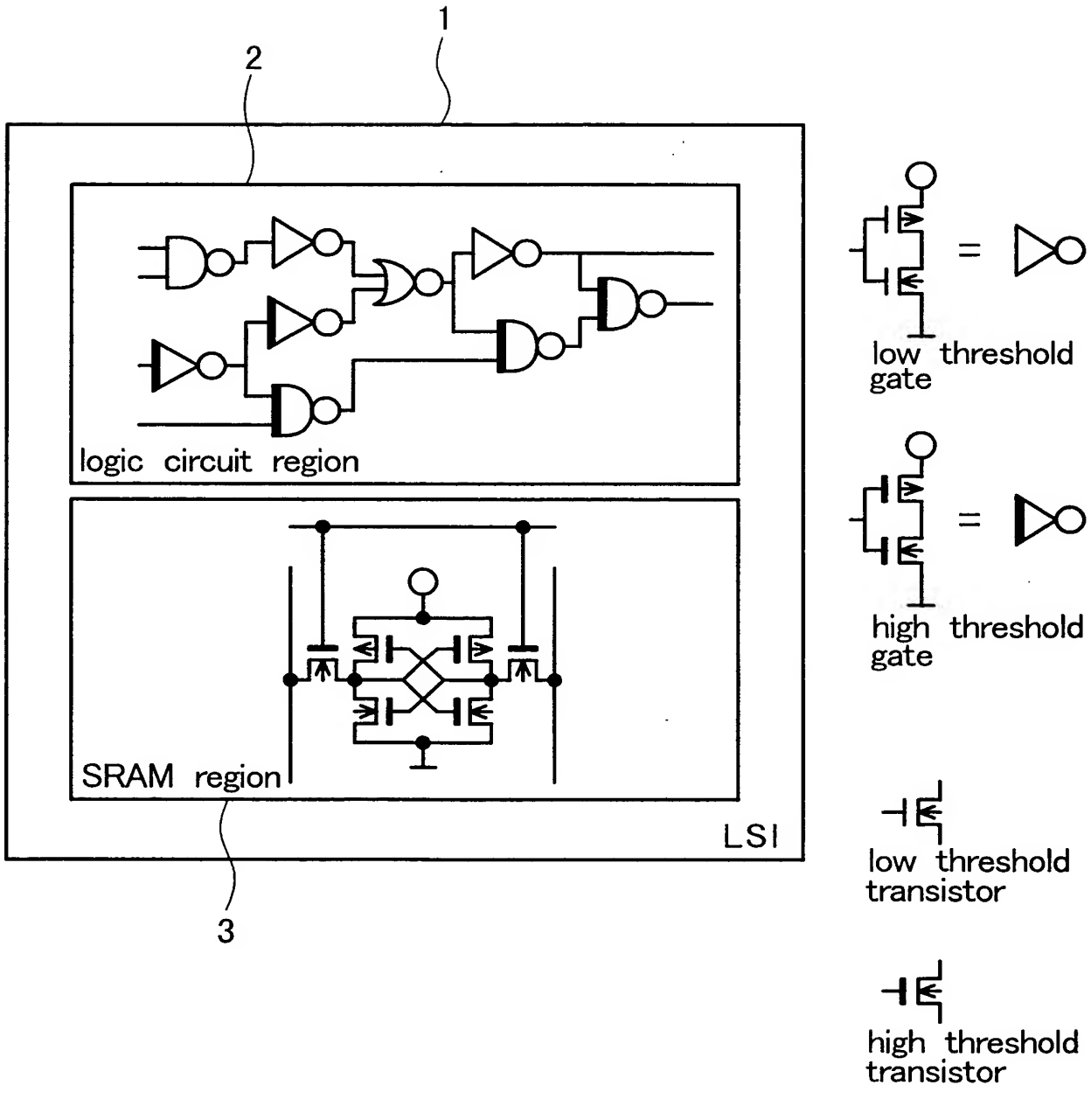

1
2
logic circuit region
SRAM region
LSI
3
low threshold gate
high threshold gate
low threshold transistor
high threshold transistor

FIG.2

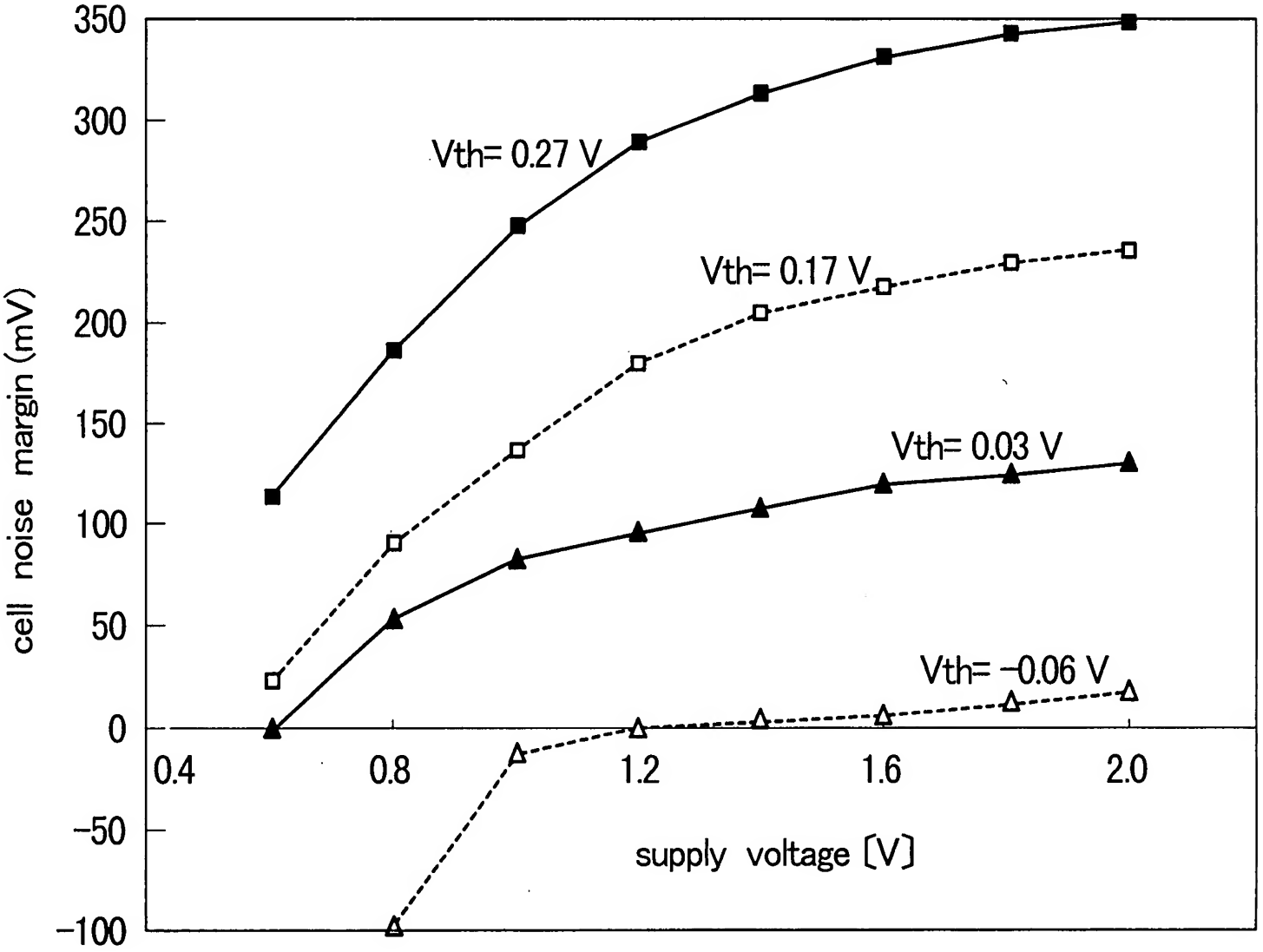

350
300
250
200
150
100
50
0
-50
-100
cell noise margin (mV)
0.4
0.8
1.2
1.6
2.0
supply voltage [V]
Vth= 0.27 V
Vth= 0.17 V
Vth= 0.03 V
Vth= -0.06 V

FIG.3

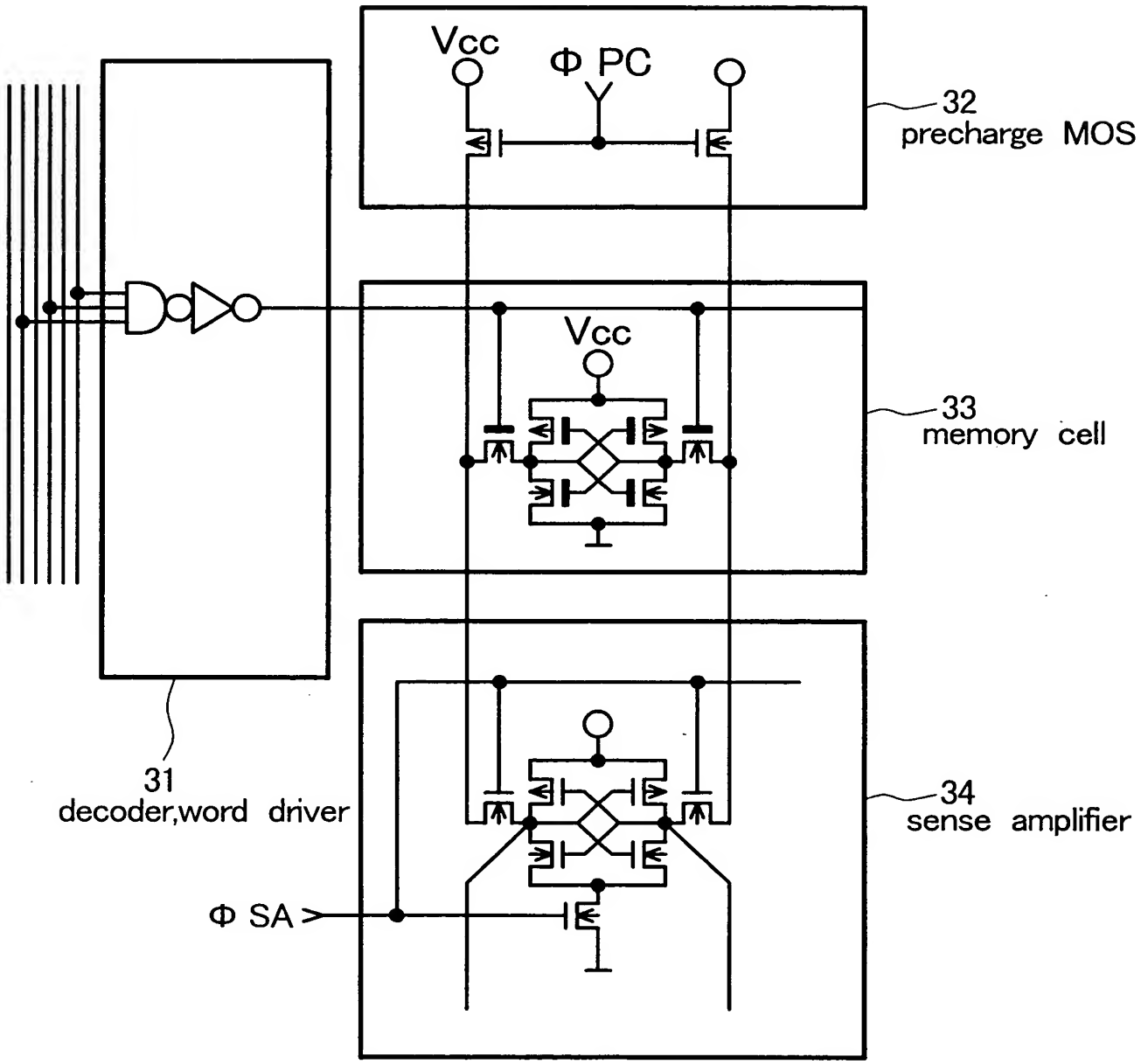

Vcc
Φ PC
32
precharge MOS
Vcc
33
memory cell
31
decoder,word driver
34
sense amplifier
Φ SA

FIG.4A

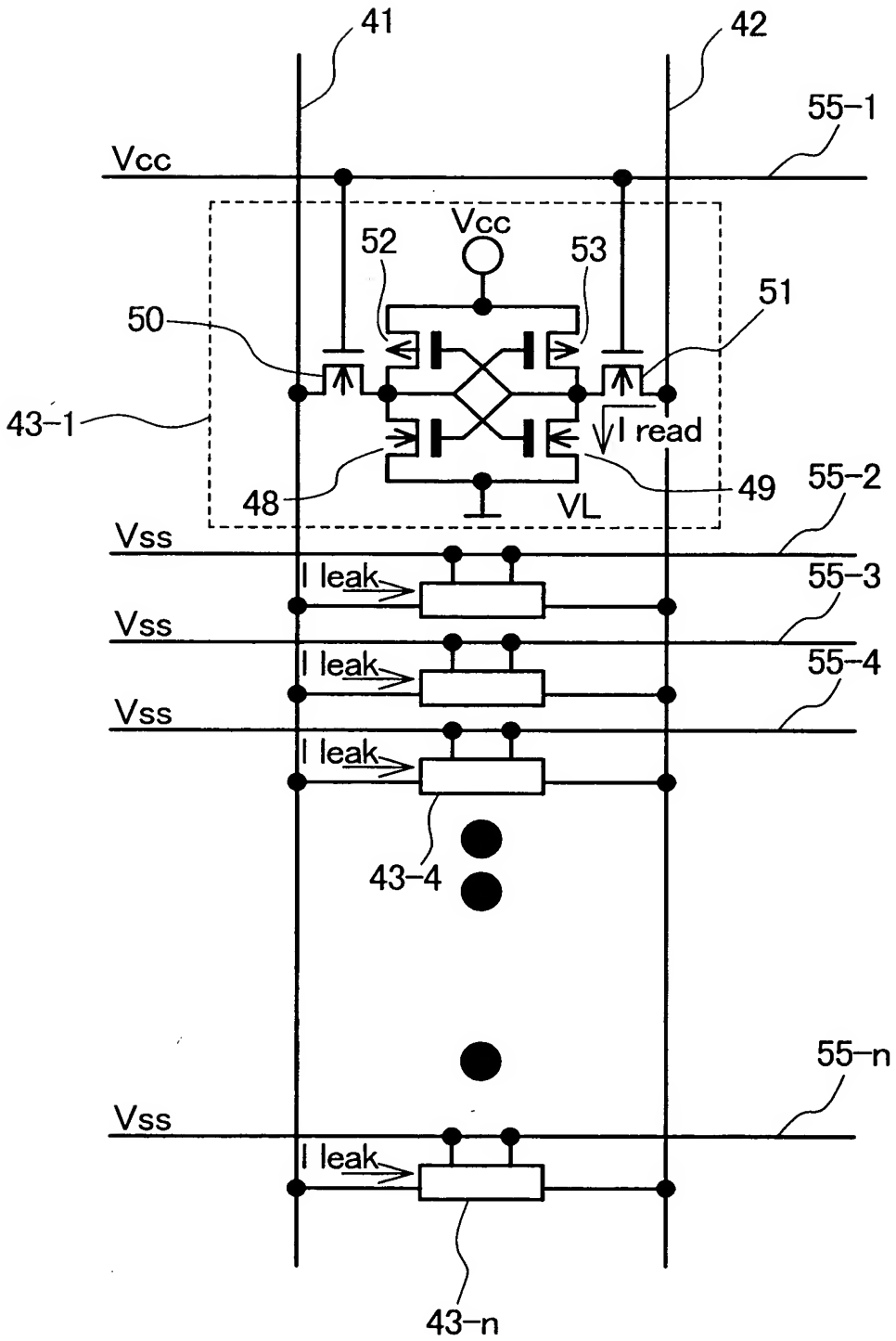

41
42
55-1
Vcc
Vcc
52
53
51
50
43-1
I read
48
49
VL
55-2
Vss
I leak
55-3
Vss
I leak
55-4
Vss
I leak
43-4
55-n
Vss
I leak
43-n

FIG.4B

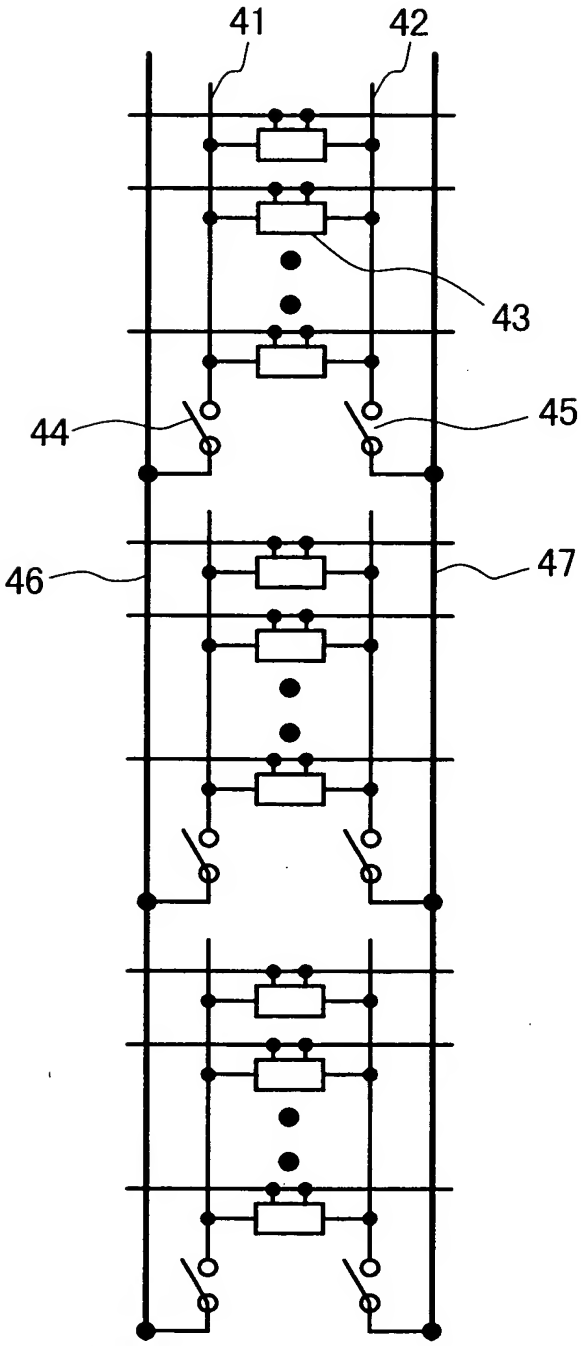


FIG.4C

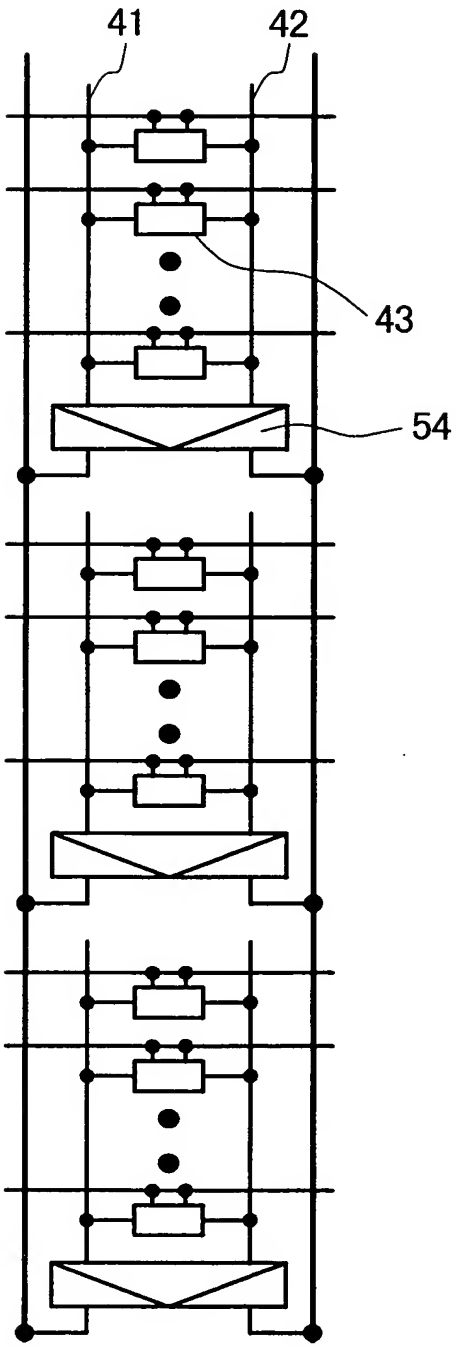
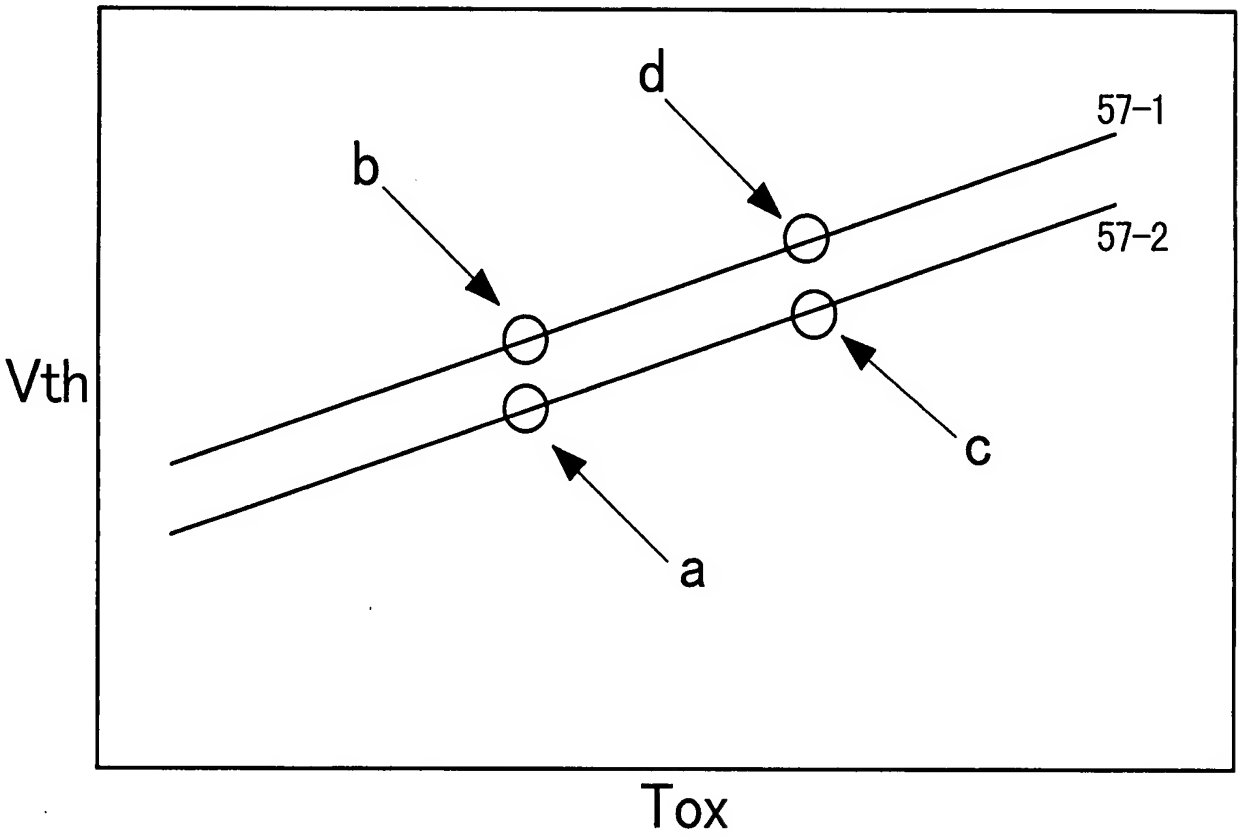


FIG.5



a low threshold transistor

b high threshold transistor

c thick low threshold-voltage transistor

d thick high threshold-voltage transistor

FIG.6

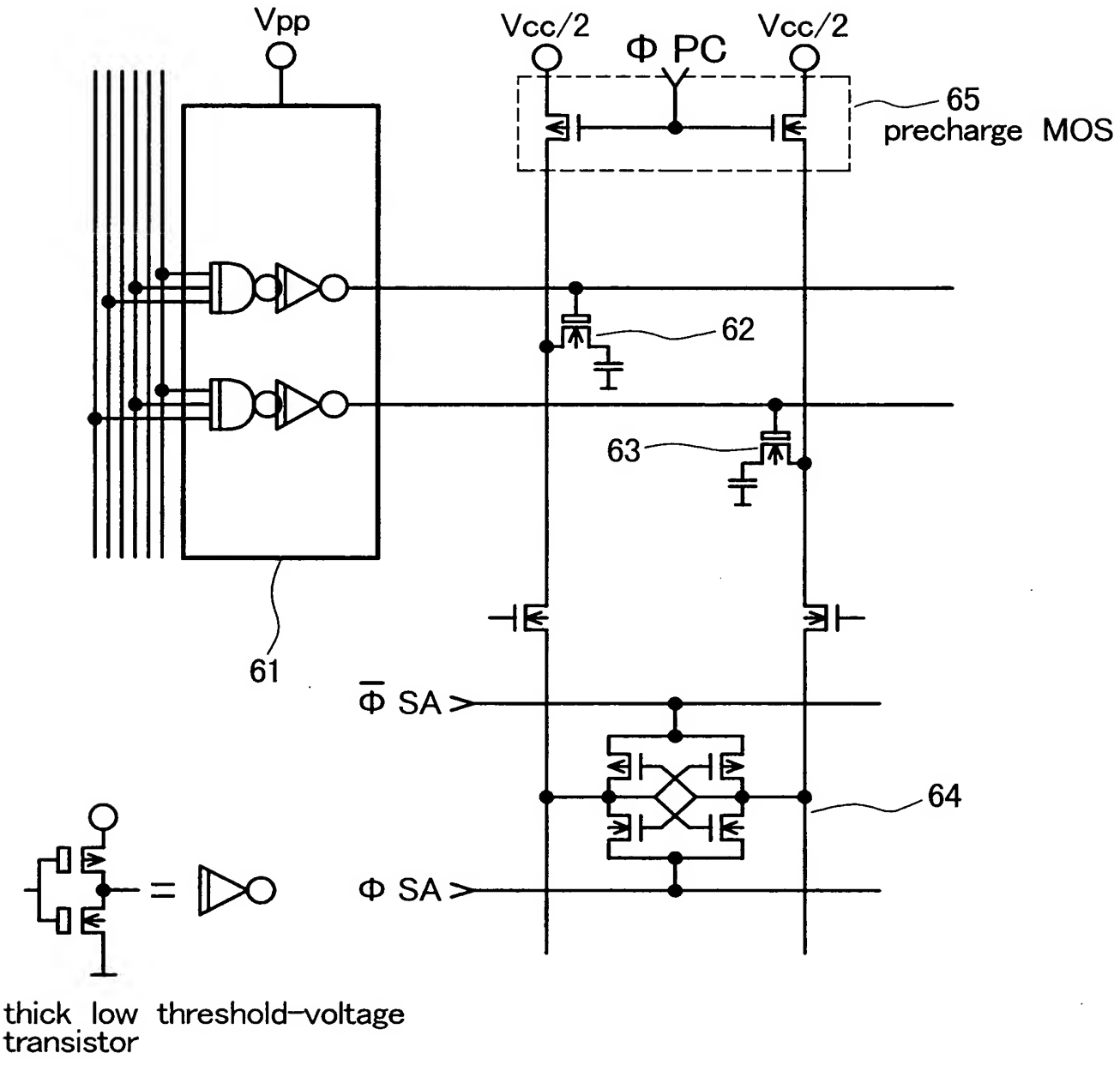

Vpp
Vcc/2
Φ PC
Vcc/2
65
precharge MOS
62
63
61
Φ SA
64
Φ SA
=
thick low threshold-voltage transistor

FIG.7

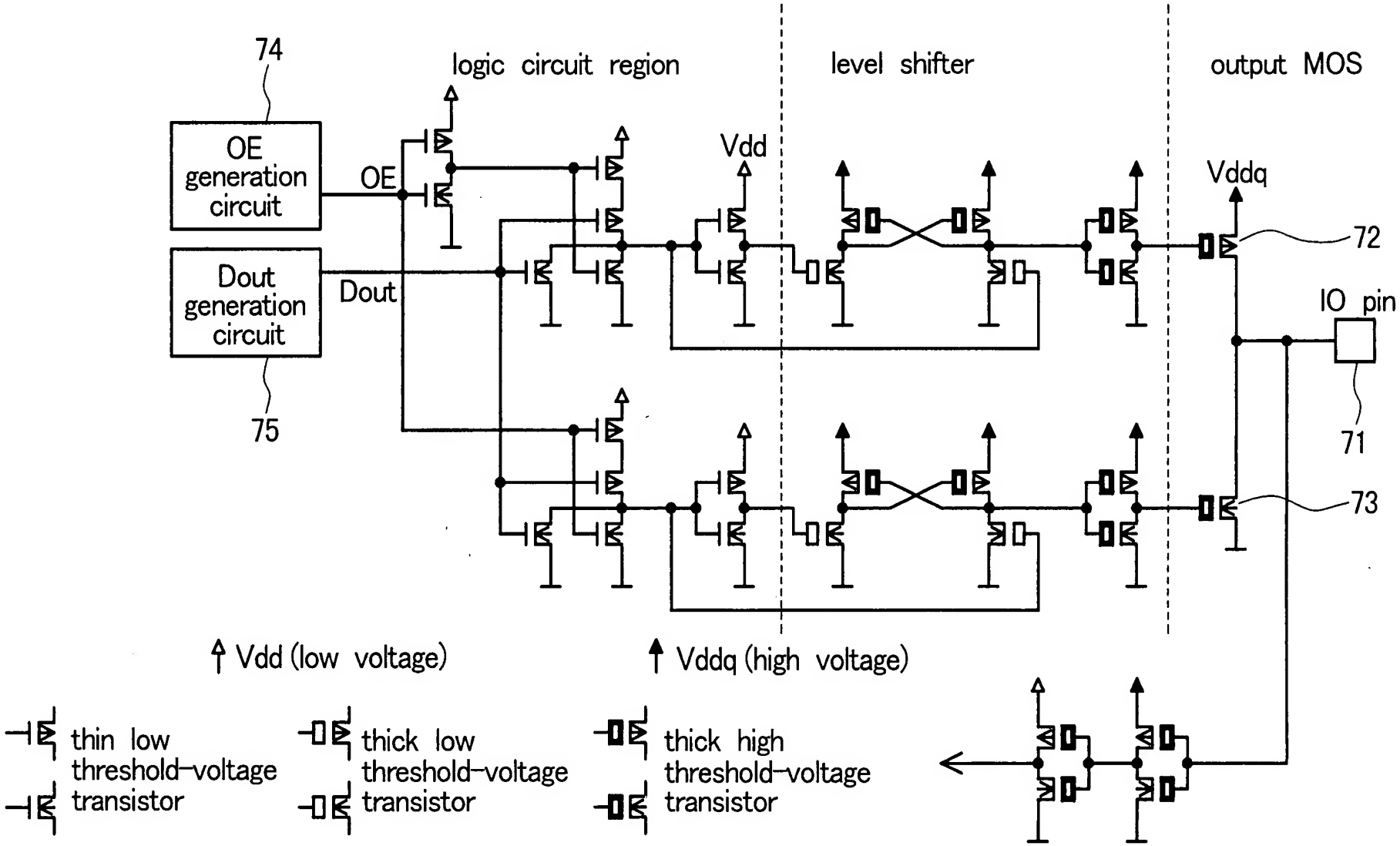
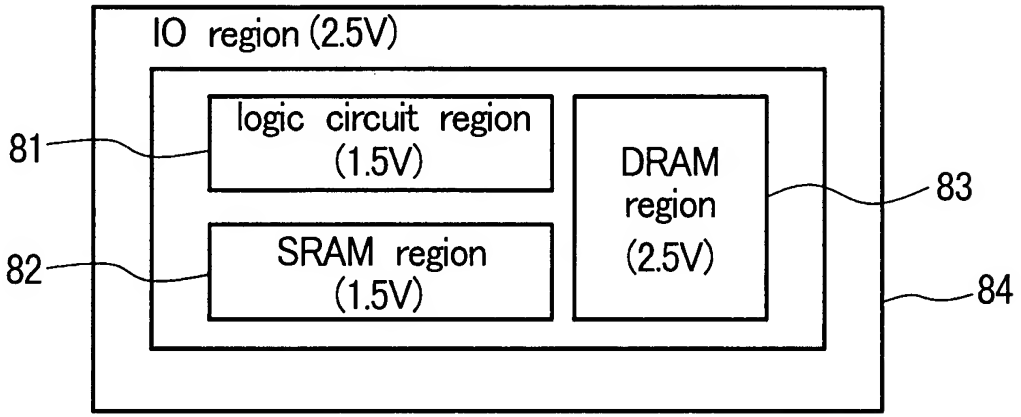

74
logic circuit region
level shifter
output MOS
OE generation circuit
OE
Dout generation circuit
Dout
75
Vdd
Vddq
72
IO pin
71
73
Vdd (low voltage)
Vddq (high voltage)
thin low threshold-voltage transistor
thick low threshold-voltage transistor
thick high threshold-voltage transistor

FIG.8



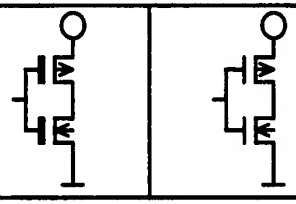
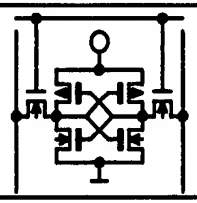
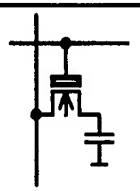
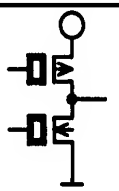
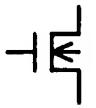
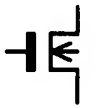
	logic circuit		SRAM			DRAM	IO
	about 90%	about 10%	load MOS	transter MOS	drive MOS	Tr MOS	
threshold voltage NMOS PMOS	high Vth (0.45V) (−0.45V)	low Vth (0.35V) (−0.35V)	high Vth (−0.45V)	low Vth (0.35V)	high Vth (0.45V)	high Vth (0.65V)	high Vth (0.65V) (−0.65V)
gate oxide	thin gate oxide (3.2nm)		thin gate oxide (3.2nm)			thick gate oxide (6.5nm)	thick gate oxide (6.5nm)
supply voltage	low voltage (1.5V)		low voltage (1.5V)			high voltage (2.5V)	high voltage (2.5V)
circuitry							
value in parentheses is an example	 thin low threshold-voltage		 thin high threshold-voltage			 thick high threshold-voltage	

FIG.9

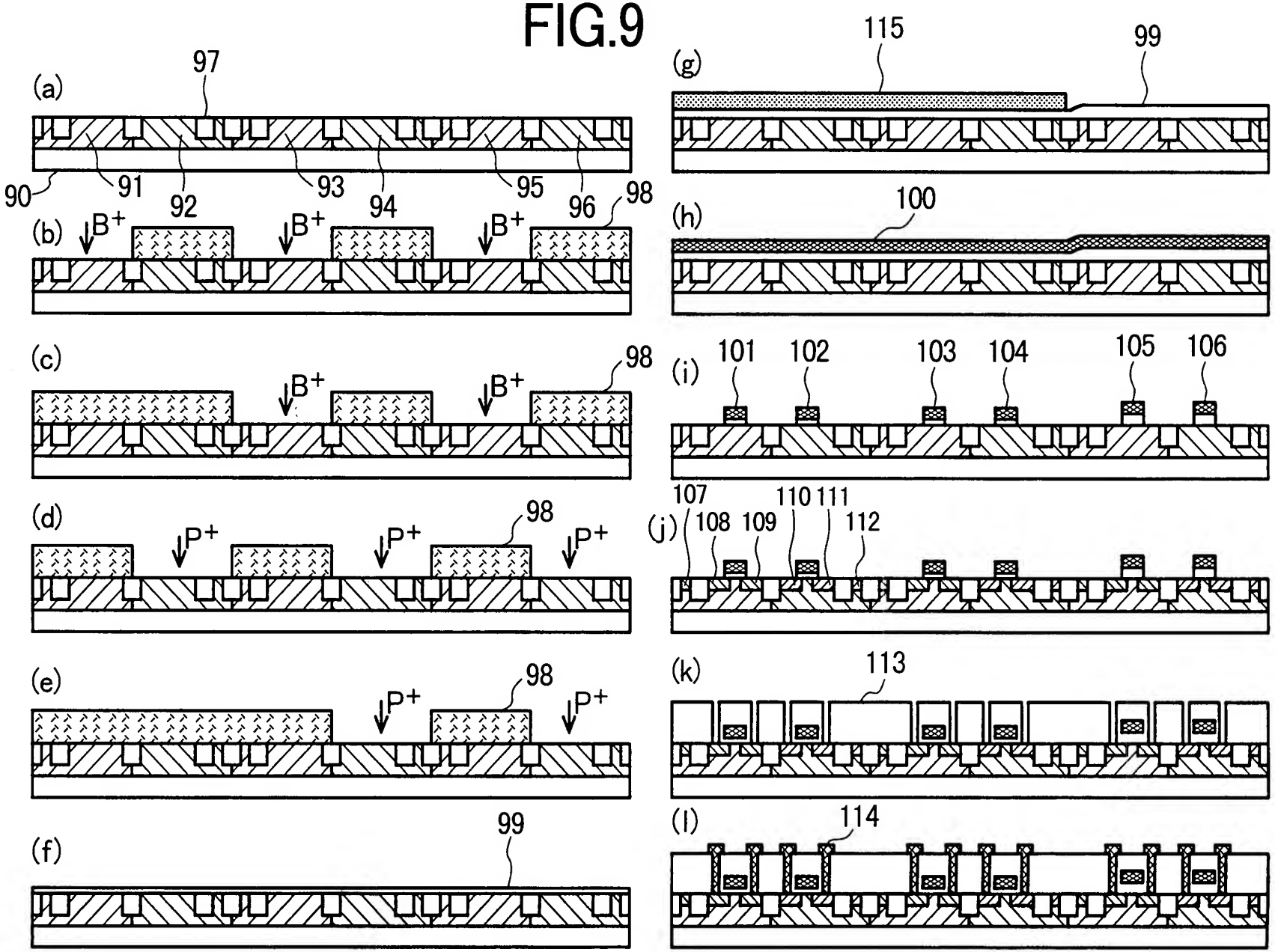

(a)
97
90
91
92
93
94
95
96
98
(b)
B+
B+
B+
(c)
98
B+
B+
(d)
98
P+
P+
P+
(e)
98
P+
P+
(f)
99
(g)
115
99
(h)
100
(i)
101
102
103
104
105
106
(j)
107
108
109
110
111
112
(k)
113
(l)
114

FIG.10

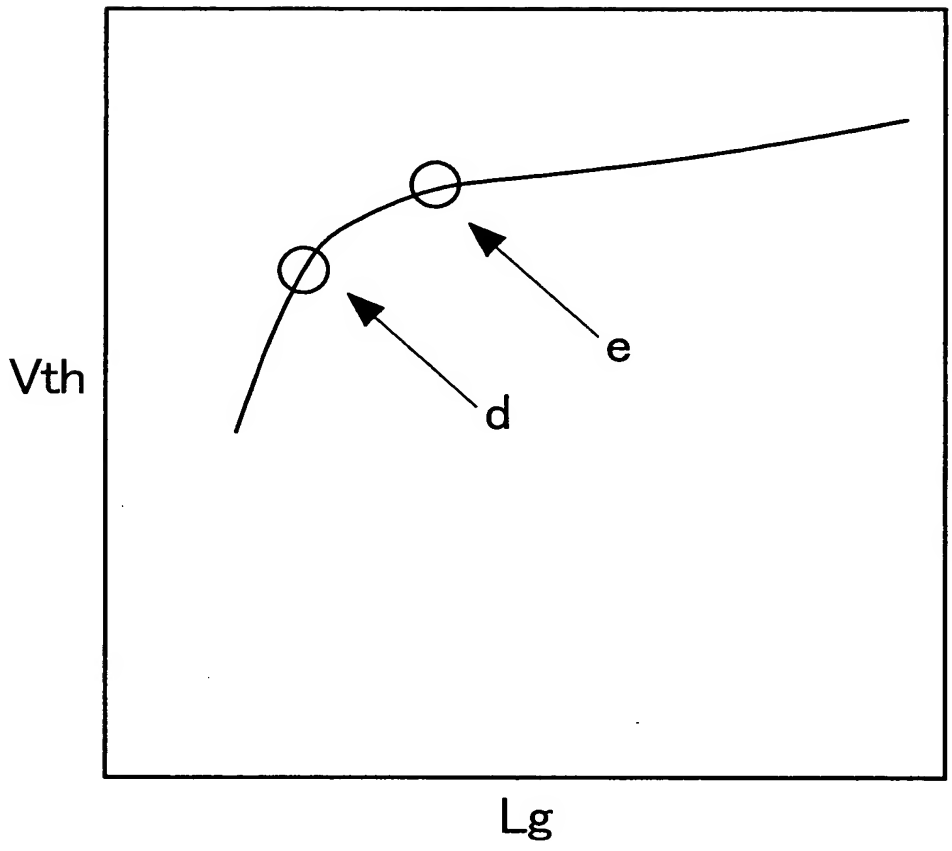


FIG.11

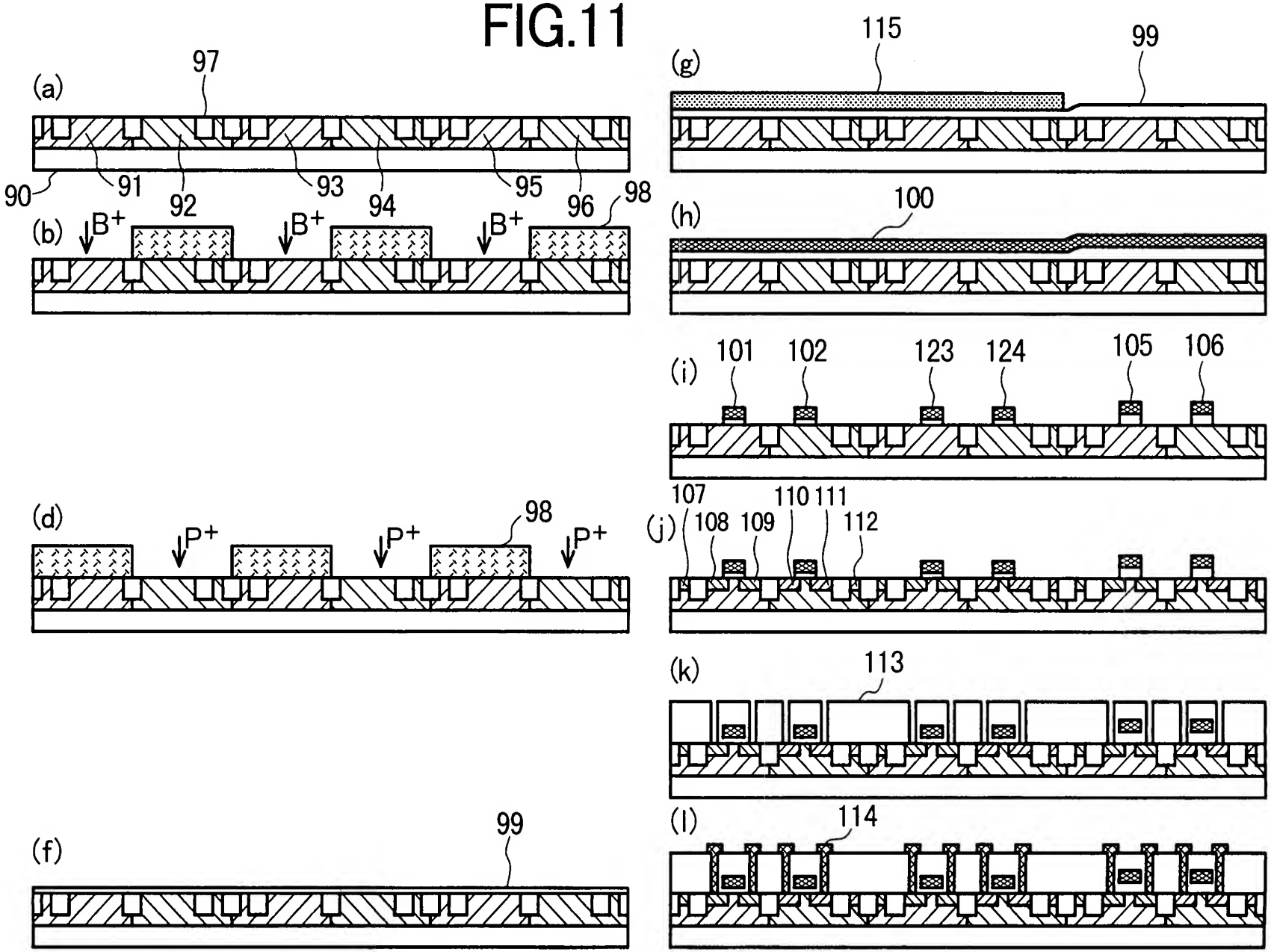
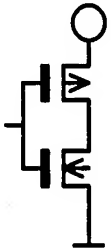
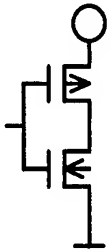
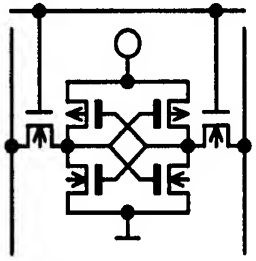
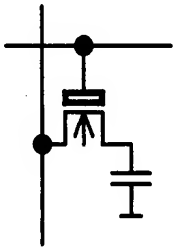
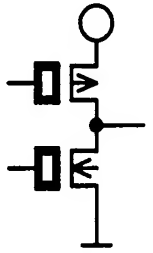
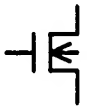
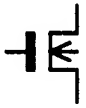

(a)
97
90
91
92
93
94
95
96
98
(b)
B+
B+
B+
(d)
P+
P+
98
P+
(f)
99
(g)
115
99
(h)
100
(i)
101
102
123
124
105
106
(j)
107
108
109
110
111
112
(k)
113
(l)
114

FIG.12

	logic circuit		SRAM			DRAM	IO
	about 90%	about 10%	load MOS	transter MOS	drive MOS	Tr MOS	
threshold voltage NMOS PMOS	high Vth (0.45V) (−0.45V)	low Vth (0.35V) (−0.35V)	high Vth (−0.45V)	low Vth (0.35V)	high Vth (0.45V)	high Vth (0.65V)	high Vth (0.65V) (−0.65V)
gate oxide	thin gate oxide (3.2nm)		thin gate oxide (3.2nm)			thick gate oxide (6.5nm)	thick gate oxide (6.5nm)
supply voltage	low voltage (1.5V)		low voltage (1.5V)			high voltage (2.5V)	high voltage (2.5V)
gate length	long channel (0.18um)	short channel (0.14um)	long channel (0.18um)	short channel (0.14um)	long channel (0.18um)	long channel (0.18um)	long channel (0.14um)
circuitry							

value in parentheses is an example

 thin low threshold-voltage

 thin high threshold-voltage

 thick high threshold-voltage

FIG.13A

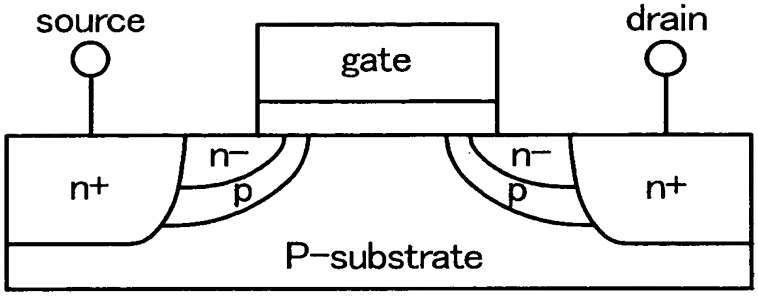


FIG.13B

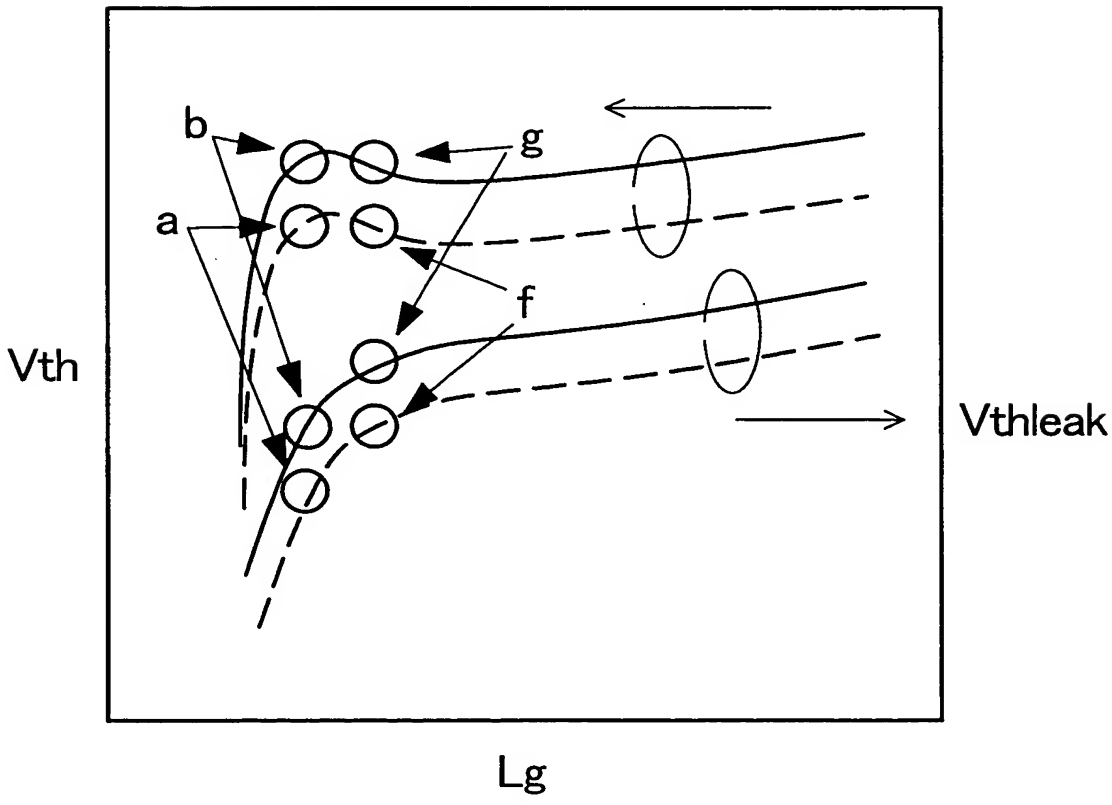


FIG.14